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AGENCY FOR INTERNATIONAL DEVELOPMENT
WASHINGTON, D.C. 20523

DATE: 8/10/87

MEMORANDUM

TO: AID/IPC/CDIE/DI, room 209 SA-18

FROM: AID/SCI, Victoria Ose VO

SUBJECT: Transmittal of AID/SCI Progress Report(s)

Attached for permanent retention/proper disposition is the following:

AID/SCI Progress Report No. C7-178

Attachment

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PD-AAW-290

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הפאקולטה להנדסה

המחלקה להתקנים וחומרים אלקטרוניים
וקרינה אלקטרומגנטית
קרית האוניברסיטה, רמת־אביב, תל־אביב 69978

TEL-AVIV UNIVERSITY
FACULTY OF ENGINEERIN

Department of Electron Devices
Materials & Electromagnetic Radiation

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PD-AAW-290

METALLIZATION AND PASSIVATION TECHNOLOGIES FOR IMPROVEMENTS IN SOLAR CELLS PERFORMANCE

A Progress Report (for 1-6/1987)
submitted to
The Agency for International Development
The U.S.-Israel CDR Program
Washington, D.C. 20523

C7-178

by

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INTRODUCTION

During the first six months of the research program we have made progress in three main directions. Firstly, starting a collaborative effort in order to merge the interests of the two groups into a comprehensive program for enhancing efficiency of solar cells. Secondly, launching a program at Tel-Aviv University, which focuses on passivation techniques for III-V compounds semiconductors. Thirdly, continuing effort in the direction of amorphous silicon thin film solar cells at the New University of Lisbon, investigating the effect of the glass substrate on the overlayer composition and the electrical conductivity. These three directions are inter-related and are elaborated below.

1. The Collaboration program

In February this year, Yoram Shapira went for a visit to Portugal to discuss the details of the collaboration program in person. This has proven to be a significant meeting because in this way we were able to specify the details of the collaboration plan, as well as to locate areas of overlapping research interests. Also, a tour of the laboratory facilities was conducted. A visit in tel Aviv by Prof. R. Martins is expected in mid-August for a couple of days. On his way to a conference in Brazil he is scheduled tostop by, visit the labs and coordinate further research plans.

We have fixed dates for the agreed exchange visits on both sides in order to transfer technologies which have matured at the Tel-Aviv University. The first visit is scheduled to take place in the middle of August for one month by a graduate student from the New University of Lisbon. During her stay of one month Miss Elvira Fortunato will be taught how to use the Auger electron spectroscopy (AES) technique in conjunction with ion sputtering. This technique is currently used by one of our graduate students who is doing his Master's degree on samples sent from Portugal. Thus the collaboration on these samples is expected to yield both analyses of these samples as well as acquiring proficiency in this technique for both students. This analysis technique is expected to be available in Portugal in the near future. Another technology to be transferred in the course of this visit is that of passivation and metallization of III-V compounds, we developed here. This is elaborated in the next section.

In September this year, a visit from a former Ph.d student from our lab is scheduled in order to collaborate with the Lisbon group on AES. This person, Dr J Bregman is an expert in this field and is expected to help our Portugese collaborators to install and run a new AES system. Thus in both exchange visits we expect a successful transfer of information about the operation and the data analysis of this technology.

The other facet of the collaboration effort is in working on samples of mutual interest such as amorphous silicon (a-Si) thin films mentioned in the previous paragraphs. These samples are fabricated in Portugal and will be analyzed in Israel using AES. Later, conclusions will be drawn by both parties in view of the experimental results, so that a joint paper is to be expected at the end of the investigation. In this way we expect to merge the expertise of

both groups into a single program, which should result in a-Si solar cells with higher efficiency and better controlled properties. The details of the samples and the planned investigation is elaborated in section 3.

2. Passivation of III-V Compound Semiconductors

I. INTRODUCTION

One of the main obstacles for obtaining reliable metal-oxide-semiconductor (MOS) devices based on III-V compound semiconductors is that a high quality passivation by native oxides has not been realized. Even though InSb is not used for solar energy conversion purposes, it was convenient for us to study it as a typical representative of its group. One workable solution for this problem, which has been successfully tried for InP [1-3], GaAs [1] and InSb [4-6], is the deposition of high quality dielectric layers directly on the semiconductor surface. Silicon oxide (silox) deposited by low temperature chemical vapor deposition (LTCVD) silicon oxide has been applied to InSb with relatively good results. As a passivation layer for InSb diodes, silox has the advantages of acceptably low deposition temperature, chemical and structural stability, a relatively simple deposition technique and transparency to visible and IR radiation. Previous studies of this subject [5-8] correlated the electrical properties with the existence of a native oxide layer at the silox-InSb interface. Okamura and Minakata [9] used bromine/methanol vapors to etch the InSb in-situ prior to silox deposition. Lower flat-band voltage (V_{FB}), hysteresis-free passivation resulted, while AES analysis did not reveal any

interfacial layer. As the main electrical feature we have used V_{FB} calculated from measured capacitance-voltage (C-V) plots.

The purpose of our study is to analyze the effect of deposition parameters and surface pre- and post-treatments on achieving improved electrical characteristics of MOS InSb devices and investigate its relationship with the existence and the chemical structure of an oxide interfacial layer.

II. EXPERIMENT

Slices of n-InSb with (111) faces were pre-etched using CP4 solution to eliminate work damage, then etched by lactic acid solution followed by buffered HF, with de-ionized water rinse between etch steps. A home-built atmospheric pressure CVD system with a bell jar type deposition chamber was used for silox deposition. Thermal post-treatment were performed in air on a controlled hot plate. Silox thicknesses were measured using Gaertner ellipsometer. Capacitance-voltage (C-V) characterization was done by an impedance meter using evaporated Au-Cr contacts. The Auger Electron Spectroscopy (AES) analyses were performed using a 3 keV, 0.5 μA, 5μm spot size electron beam and a single-pass cylindrical mirror analyzer. In depth analysis was done with a rastered grazing incidence ion gun producing a 1 keV and 0.15 μA Ar^+ ion beam. A quantitative Auger Electron Spectroscopy (AES) method, which was developed earlier by our group [10-11], was implemented.

III. RESULTS

The passivation process is composed of three sequential main stages, namely: The semiconductor substrate pre-treatment, the passivation film growth, and its post-treatment. We tried to correlate V_{FB} to the specific parameters or detailed process of each stage.

1. InSb Pre-treatment.

As explained above, the InSb surface "standard" pre-treatment includes CP4 chemical polishing; chemical etching, with lactic acid solution; and finally surface oxide etch with hydrofluoric acid (HF). Several variations and additional steps were tried in order to study their effects on V_{FB} and on the interface trap density Qss/q.

Table 1

InSb SURFACE PRE-TREATMENT EFFECT ON V_{FB} AND Qss/q for 0.1 μm THICK SiO_2 LAYERS

Pre-treatment procedure	V_{FB}(Volts)	Qss/q(cm^{-2})x10^{-11}
"Standard" procedure	(-0.1)-(0.1)	1-1.2
"Standard" except for omission of HF etch	(-0.5)-(-1.2)	1.9-3.2
"Standard" except for omission of lactic acid solution etch	(-0.1)-(-0.3)	1.1-1.3
"Standard" plus an extra methanol rinse	0.3	0.5

Table 1 summarizes the effect of several such treatments. The variations for each treatment in the tabulated values refer to lateral inhomogeneity. One clear finding from Table 1 is that an additional methanol rinse following the HF etch decreases the passivation layer positive charge. Also, V_{FB} can notably be a positive as +0.5 volts. Bearing in mind that the calculated ϕ(Au-Cr/InSb) = - 0.5 volts, this implies a zero net charge in the passivation layer. Another finding is that the omission of HF etch causes wide lateral variations in V_{FB}. Omission of the lactic acid solution etch has only a minor effect increasing both V_{FB} and its lateral nonuniformity.

2. Effect of Deposition Parameters

The effects of the deposition stage were studied on samples which had all undergone the "standard" surface preparation. The deposition parameters were modified relative to a standard set of conditions, namely, gas flow rates: N_2 - 4ℓ/min, 5% SiH_4 - 100 cc/min, O_2 - 10 cc/min, substrate temperature, T = 250C and system pressure P = 2.5 inches of water. Among these parameters only the temperature and the pressure were found to have a significant effect on V_{FB}. Figure 1 illustrates the effect of the substrate temperature. While for T > 235C V_{FB} is independent on temperature, it decreases at T < 235 C. However, below 230°C the deposition rate decreases to a negligible rate. Figure 2 illustrates the pressure effect. At zero pressure V_{FB} is at its highest value and it decreases with increasing pressure up to about 2 inches of water, beyond which it does not vary anymore with pressure.

3. Thermal Treatment

Low temperature, ambient air post-treatment of the samples was found to cause a decrease in V_{FB}. Figure 3 illustrates the time dependence of this effect, for 80C. All measurements were done during the first day following heat treatment for the indicated number of days. V_{FB} is seen to decrease with heating time quite steeply, and to go through a minimum value at the second day of treatment, following which it slowly increases with heating time. The V_{FB} value during shelving time following a heat treatment is not stable. As shown in Figure 4, which describes V_{FB} as a function of shelving time in vacuo after 3 days of heat treatment at 80 C, it decreases first and then stabilizes at V_{FB}s corresponding to Qss/q close to zero (+0.5 v). Two mechanisms seem to combine at the annealing stage. The first one dominates during the treatment, the second is concurrent but can go on even when the treatment is over. C-V plots of two samples, before and after heat treatment, are shown in fig. 5. Besides the large shift in V_{FB}, additional differences can be observed between the two. After the heat treatment the C-V curve exhibits higher slope in the depletion region and narrowing of the hysteresis. Both changes are indicators of general improvements in the interface characteristics. The former points to lower "fast" interface trap density and the latter to lower "slow" trap density.

4. AES Analysis

Analysis of AES results was expected to yield information about the composition of the silox film and about the existence, the width and the chemical composition of an interfacial layer underneath it. Four samples were used for this purpose: Sample #1 which underwent the "standard" pre-treatment and deposition procedures; sample #2 for which the HF acid pre-etch step was omitted with the result of increased (more negative) V_{FB}; sample # 3 which was rinsed in methanol following the final DI water rinse and prior to deposition, with the result of a decreased (more positive) V_{FB}; and sample # 4 which went through 3 days of heat treatment in air which resulted again in improved V_{FB}.

We followed the variation vs. depth of Sb peaks at energies of 453 eV and 461 eV, of In peaks at 400 eV and 407 eV, Si at 78 eV and O at 510 eV. An extra Si peak at 88 eV which is close to the elemental Si line (at 93 eV) was observed in all four silox/InSb samples. This interesting observation indicates the existence of SiO_x in an incomplete state of oxidation, which is the product of the deposition technique. A depth profile of a thermal Si oxide under identical analysis conditions did not reveal such a component, thereby convincing us that our observation had not been an artifact of the sputter-AES method. Furthermore, IR absorption measurements were performed on 0.1 μm-thick silox on high resistivity Si substrate. A resulting spectrum is given in fig. 6, which shows, besides SiO_2, an absorption peak at 880 cm^{-1}. This peak is attributed to Si_2O_3.[11] It was also observed by Langan,[6] who reported its disappearance at higher silox deposition temperatures. The Si in its incomplete oxidation state may also contribute to charges and traps within the oxide.

Sputtering through the silox, we eventually encounter an intermediate layer where both Si lines decrease while In and Sb lines increase. This is well shown in figs. 7 and 8, which are AES calibrated depth profiles of 0.1 μm thick SiO_2 interfaces with InSb. Fig. 7 was taken from a sample that had undergone the standard surface treatment. The extended interface is clearly seen. Fig. 8 shows a profile of a sample after heat treatment, which shows a somewhat reduced interface width. A methanol rinse before silox deposition produces a profile similar to the one shown in fig. 8.

The widths of the interface layers are tabulated in Table 2 which also indicates V_{FB} for each sample. In sample no. 2, the In "tail" into the silox extends about 200-300 Å beyond that of the Sb. This suggests that the native oxide formed following the lactic acid solution etch has a high In:Sb ratio. The In species may play an important role as an electron trap. The HF etch seems to improve the surface stoichiometry prior to deposition. The interface layer of sample no. 3 is about half the width of the other three. This may point to the role of methanol in dissolving ionic In and Sb species left on the surface and thus in improving V_{FB}.

The most significant observation seems to be that for each sample the Si lines at the interface inner edge disappear before to the decrease of the oxygen concentration to zero. Thus, the area which includes O, In and Sb peaks suggests a native oxide interlayer. The widths of these layers are also tabulated in Table 2. It clearly shows that decreased interlayer widths are caused by both the methanol pre-treatment and the thermal post treatment together with a decrease in V_{FB}. The correlation between interface, oxide-layer thickness and V_{FB} can be explained by a simplified model which considers

a uniform distribution of the interface changes in the native oxide interlayer and thus their surface concentration increase with this oxide thickness.

Table 2

RELATION OF INTERFACE AND NATIVE OXIDE LAYER WIDTHS WITH V_{FB} VALUES FOR 0.1 μm THICK SiO_2 LAYERS ON InSb

Sample number	Treatment	V_{FB}(v)	Interface width (Å)	Native oxide wi (Å)
1	Standard	(-0.1)-(0.1)	300	70
2	HF omission	-1.1	300	100
3	Methanol rinse	(0.3)-(0)	160	30
4	Heat treatment	(0.2)-(0.4)	250	30

Although the interface width may be partially attributed to sputtering-redistribution and surface roughness, the correlation of the V_{FB} valu the corresponding native oxide layer widths points out the role of the l

IV. DISCUSSION AND CONCLUSIONS

V_{FB} of silox/InSb MOS capacitors was found to be dependent on the detailed InSb surface pre-treatment, specifically, an additional methanol rinse; on two deposition parameters, namely - substrate temperature and deposition pressure; and more strongly, on thermal post-treatment. AES

analysis proved the existence of diffuse InSb/silox interfaces with a thickness of the order of several hundred Å and at the interface with the InSb substrate a native oxide layer, 30 to 120 Å thick, which is in accordance with previously reported works.[9-10] The thicknesses of these layers correlate well with V_{FB} values for the analyzed samples. A simplified model can be thought of in which charges in the native oxide are responsible for at least part of Qss, and that the concentration of these charges is directly related to the native-oxide thickness. Along this line all substrate pre-treatments which are found to affect V_{FB} could be explained in view of their effectiveness in leaving an oxide-free surface prior to deposition. The positive effect of an additional methanol rinse following the HF etch might be due to its role as a solvent for various ionic species of In and Sb left on the surface. It could also act as a solvent for adsorbed residual water vapor. Adsorbed water may be an additional source of surface oxidation during the heating state in the deposition chamber.

The positive effect of deposition pressure on V_{FB} may be through its effect on the completion of the oxidation reaction in the gas phase prior to the heterogeneous stages of the overall deposition reaction. This possibility agrees well with the model suggested by Langan [5-6]. In this model the native oxide is the key for low surface charge density. This reasoning could still be applied in our case if we suppose that there is an optimum thickness and composition for the native oxide. When its thickness increases the charge density would increase.

The heat treatment decreases V_{FB} while AES results show again a narrower native oxide layer. Thus, the effect may be due to more complete oxidation of In and Sb, which, in their elemental form, are believed to be sources for interface trapping. The seemingly surprising narrowing of the native oxide interface can be thought of in terms of different oxidation potentials of the

participating species, as well as as interdiffusion at the silox-native oxide interface.

The extent and effect of cation and anion (differential) diffusion into the silox layer and its possible effect on the silox positive charge is still under progressive study. These results would hopefully shed more light on the various components of silox/III-V compound semiconductor system. The paper described above was sent to the Journal of Applied Physics for publication with a proper acknowledgement to the U.S. A.I.D.-C.D.R. Program for your support.

3. Deposition of a-Si Thin Films

In the course of fabrication of a-Si, and indium-tin-oxide (ITO) thin films on glass substrates it was found that they have a tendency to "leach" various contaminants from the substrates. These contaminants comprise mostly of Na ions which prevail in most commonly used glasses and being small and highly mobile can easily diffuse into the overlayer. These contaminants affect the electrical conductivity of the overlayer. In order to avoid this problem one should use Na free substrates or devise diffusion barriers between the substrate and the overlayer. As a first step, efforts are being made to establish the leaching process. Secondly, the type of contaminant will be determined and the possibilities include Na, C, F, H, N and O. The effect on the electron conductivity will be determined by I-V measurements as well as by chemical composition measurements using AES, as described in section 1. Thirdly, the different effects of the contaminants will be determined as a function of the overlayer material and its type and level of doping. When this

data is analyzed we hope to be able to reach conclusions about the best way to go about solving this problem. If we can change the substrate to one which is free of contaminants that will obviously be the simplest way. However, if this cannot be done we will have to launch a new program of looking into suitable interlayers, which will act as diffusion barriers. These interlayers (e.g. SiC) need to have two specific features, they have to completely block diffusion of contaminants from the underlying substrate into the film and they have to be thin enough and with suitable electrical characteristics as not to interfere with the device performance. Such directions have been used in our laboratory of the Tel-Aviv University and we hope to be able to help in this direction if necessary.

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FIGURE CAPTIONS

Fig. 1. V_{FB} of InSb MOS capacitors with 0.1 μm thick SiO_2 layers as a function of substrate temperature during deposition.

Fig. 2. V_{FB} of InSb MOS capacitors with 0.1 μm thick SiO_2 layers as a function of gas pressure during deposition.

Fig. 3. V_{FB} of InSb MOS capacitors with 0.1 μm thick SiO_2 layers as a function of duration of heat treatment in ambient air at 80C.

Fig. 4. V_{FB} of InSb MOS capacitors with 0.1 μm thick SiO_2 layers as a function of shelving time following 3 days of ambient air, 80C heat treatment. Original V_{FB} value of as deposited capacitor is also indicated.

Fig. 5. C-V of a typical InSb MOS capacitor with 0.1 μm thick SiO_2 layer before (dashed line) and after (solid line) heat treatment at ambient air, 80C.

Fig. 6. IR absorbance spectrum of silox/InSb showing a peak at 1065 cm^{-1} attributed to SiO_2 and a peak at 880 cm^{-1} attributed to Si_2O_3 .

Fig. 7. AES calibrated depth profile of an interface of a 0.1 μm thick S_2 .

layer on InSb. The sample had undergone the standard surface treatment before silox deposition. The profile shows Si peaks (in SiO_2 and SiO_x), O, In and Sb peaks. The intensities of the last two coincide.

Fig. 8. AES calibrated depth profile of an interface of a 0.1 μm thick SiO_2 layer on InSb. The sample had undergone the standard surface treatment before silox deposition and was then subjected to 80 C heat treatment.

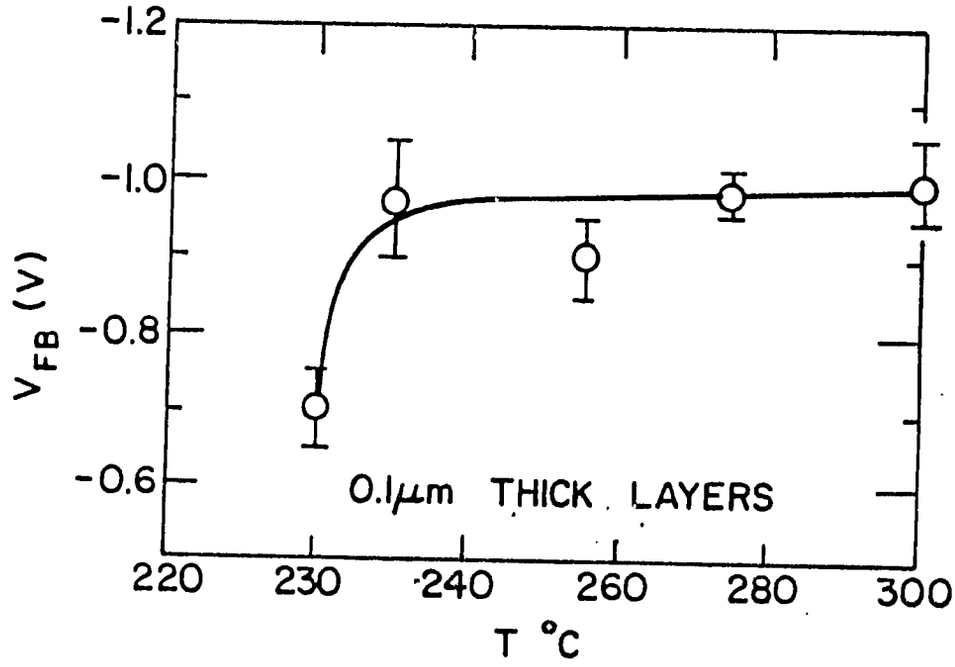
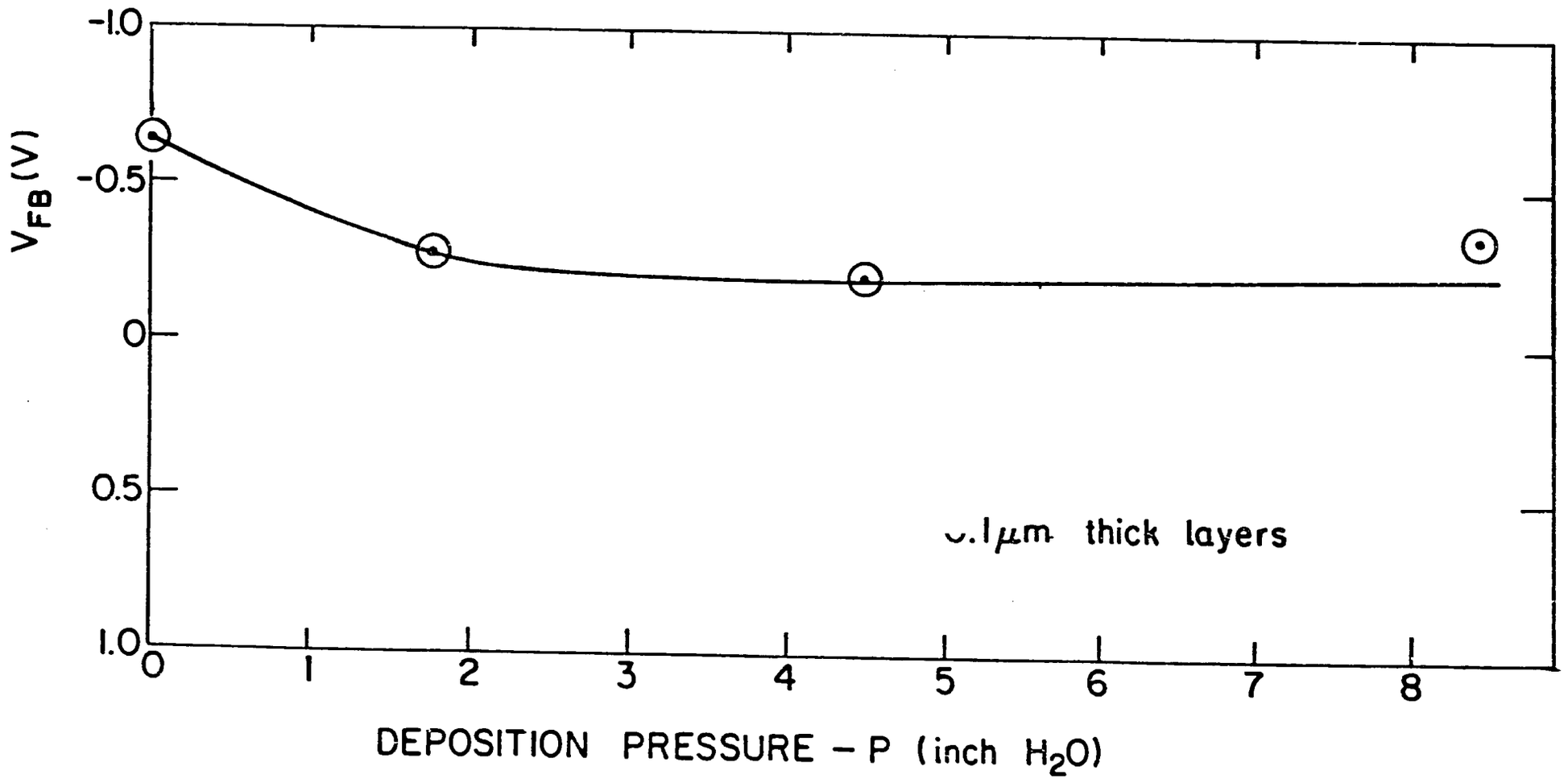


FIG. 1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V_{FB} (V)
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2
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4
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7
8
DEPOSITION PRESSURE – P (inch H_2O)
0.1μm thick layers

Fig. 2

19.

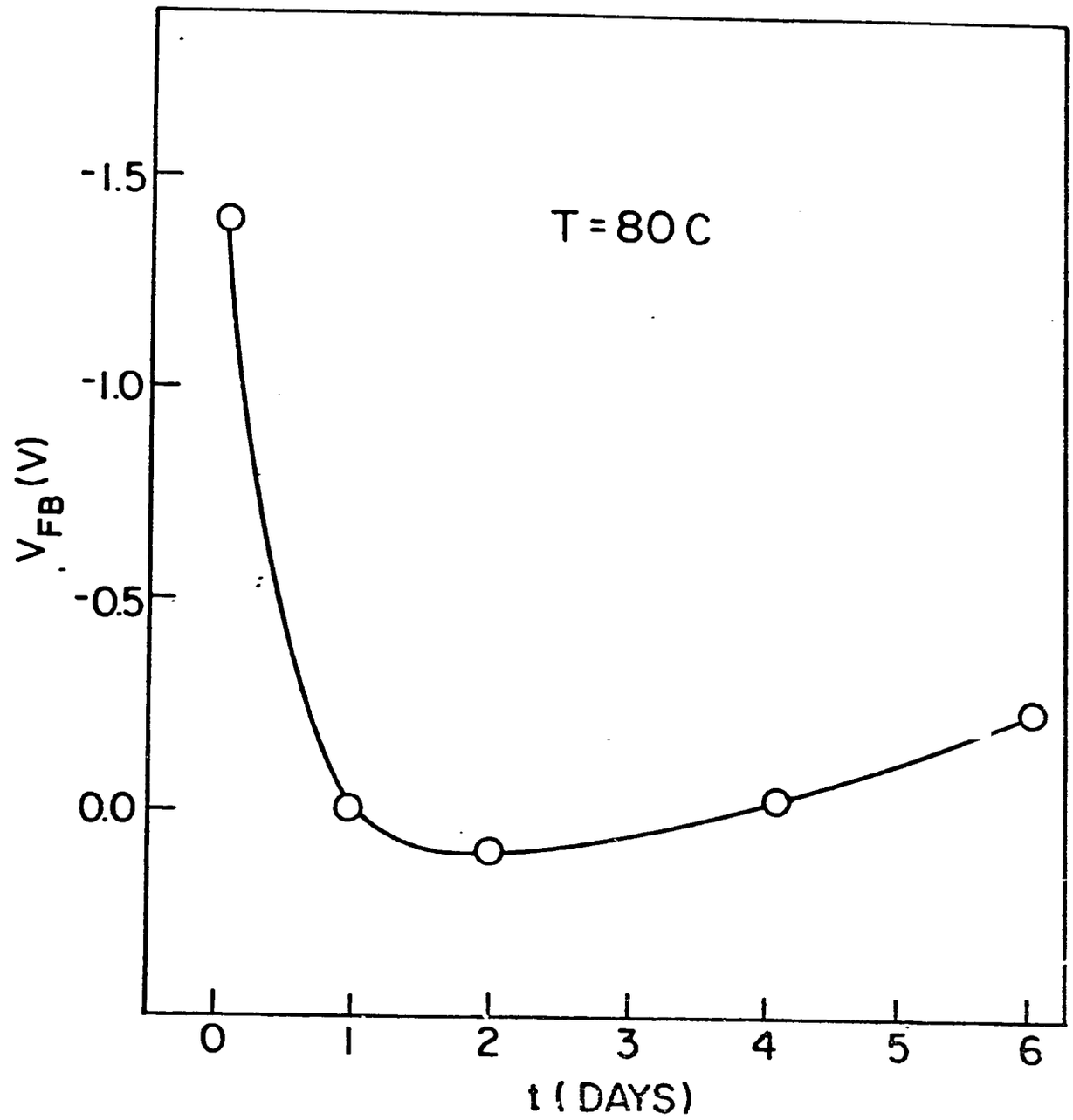


Fig. 3

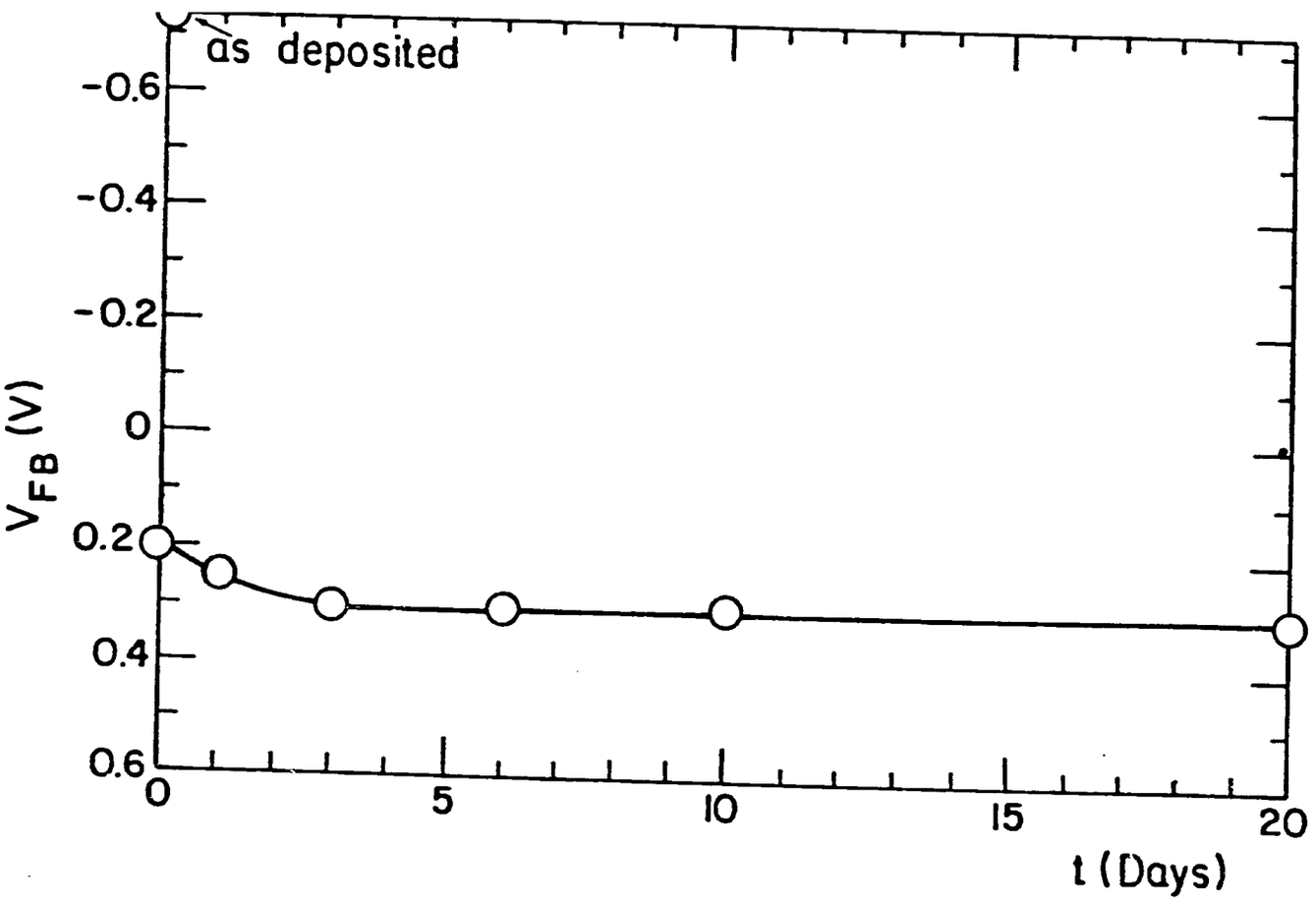
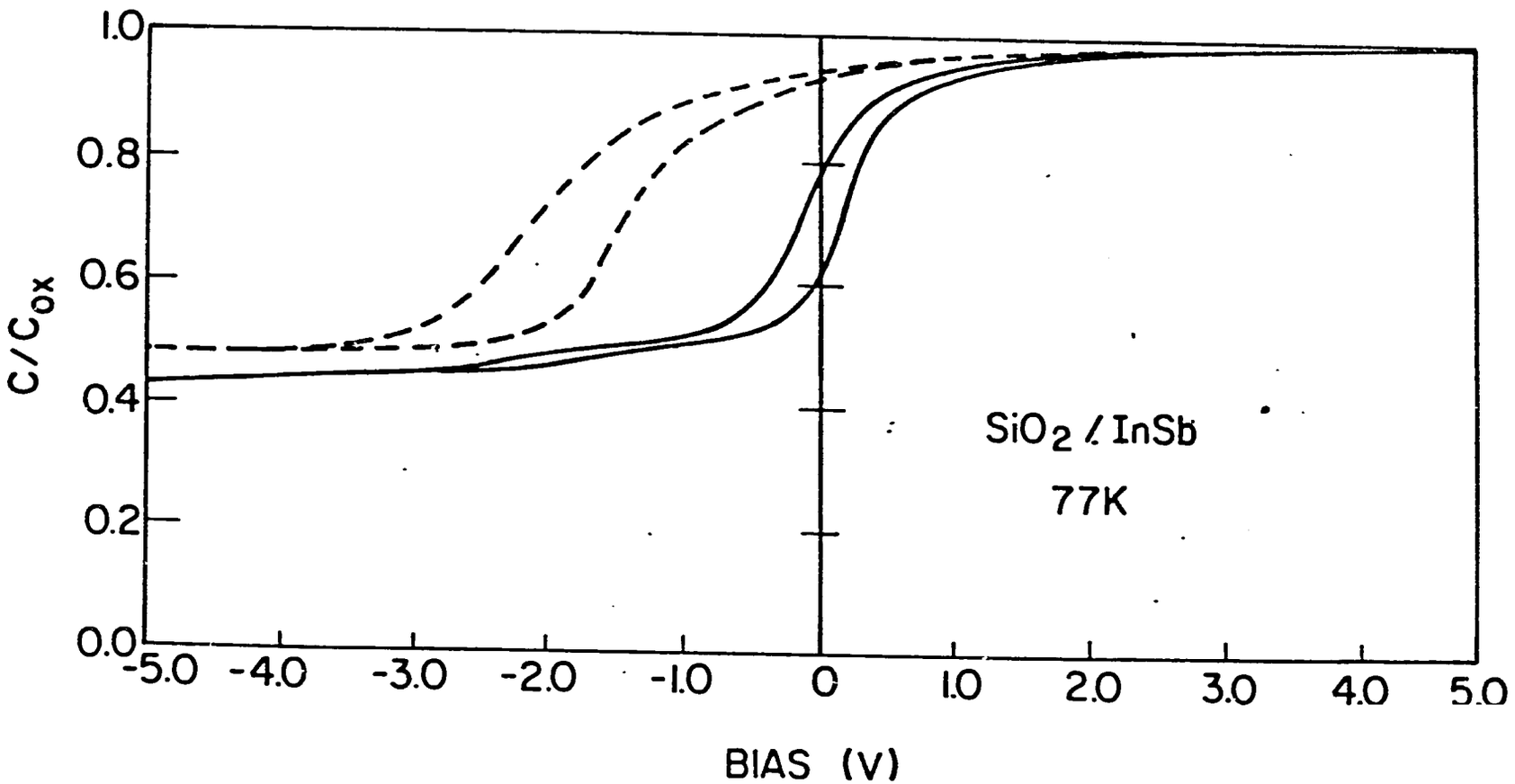


Fig. 4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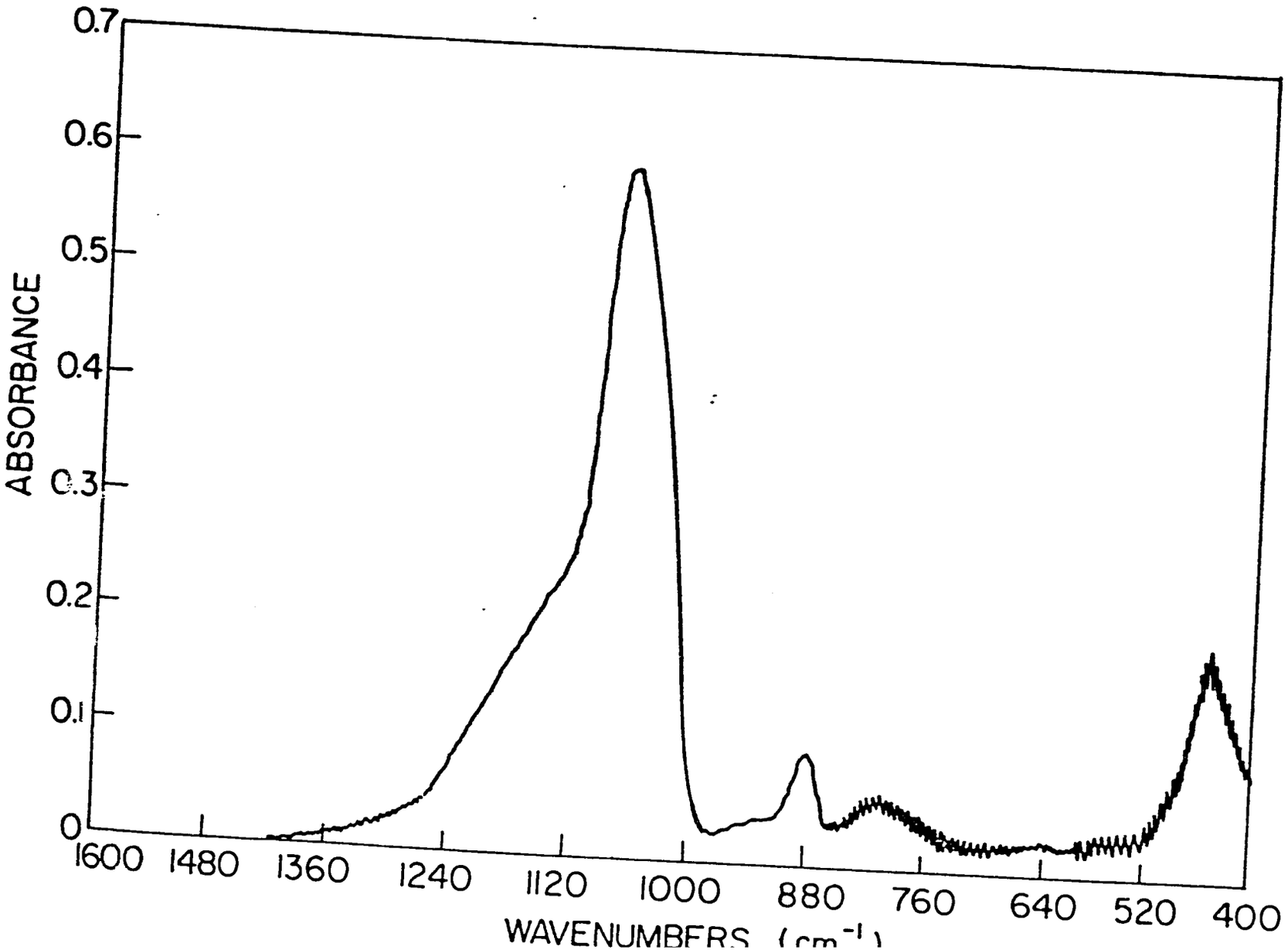
BIAS (V)
SiO2 / InSb
77K

Fig. 5

22

Fig. 6.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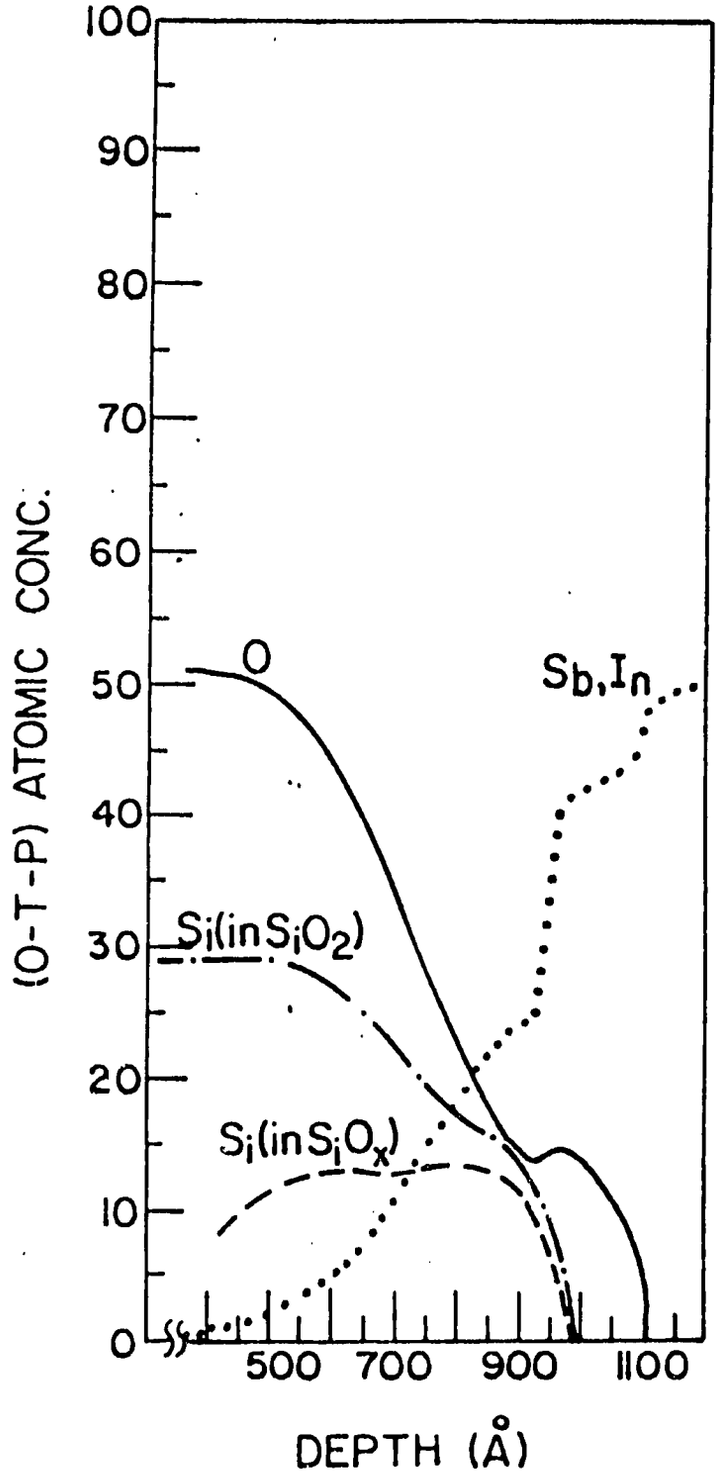
400
WAVENUMBERS (cm⁻¹)


100
90
80
70
60
50
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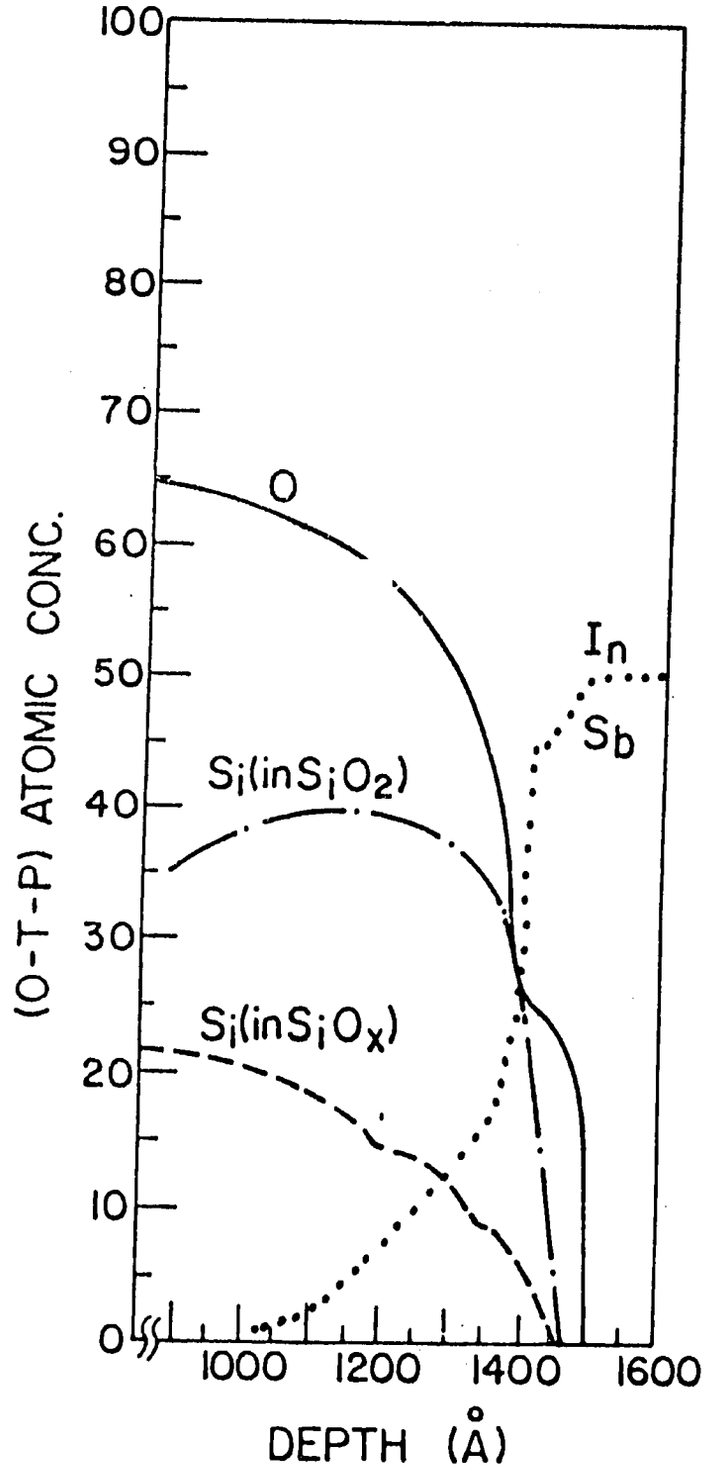
10
0
(O-T-P) ATOMIC CONC.
O
Sb, In
Si(in SiO2)
Si(in SiOx)
500
700
900
1100
DEPTH (Å)

Fig. 7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DEPTH (Å)

Fig. 8